IN THE CLAIMS

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims:

1. (Currently amended) A computer system comprising:

a processor;

a memory controller coupled to the processor;

a memory coupled to the memory controller;

a first input/output (I/O) controller coupled to the memory controller;

a first expansion slot coupled to the first I/O controller; and

a test module card directly coupled to the first expansion slot;

wherein the test module card is configured to obtain access to a portion of the memory from an operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

2. (Currently amended) The computer system of claim 1 further comprising:

~~an~~ the operating system;

wherein the processor is configured to cause the operating system to be booted, and wherein the test module card is configured to cause the tests to be performed on the portion of the memory ~~using the first bus~~ subsequent to the operating system being booted.

3. (Currently amended) The computer system of claim 1 further comprising:

~~an~~ the operating system;

wherein the processor is configured to cause the operating system to be executed, and wherein the test module card is configured to cause the tests to be performed on the portion of the memory ~~using the first bus~~ during execution of the operating system.

4. (Original) The computer system of claim 1 further comprising:
a second I/O controller coupled to the memory controller;
a second expansion slot coupled to the second I/O controller; and
an I/O device coupled to the second expansion slot.

5. (Original) The computer system of claim 1 wherein the test module card is configured to cause tests to be performed on the memory by providing read and write transactions to the first I/O controller.

6. (Original) The computer system of claim 5 wherein the read and write transactions comprise DMA transactions.

7. (Original) The computer system of claim 1 further comprising:
a bus bridge coupled to the processor and the first I/O controller.

8. (Original) The computer system of claim 1 further comprising:
a system controller that comprises the memory controller.

9. (Currently amended) A method comprising:
~~selecting~~ obtaining access to a portion of a memory of a computer system from an operating system ~~for testing~~ during operation of ~~the~~ a computer system;
generating a test transaction in a test module card directly coupled to an expansion slot of the computer system; and
providing the test transaction to the portion using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

10. (Original) The method of claim 9 further comprising:
detecting an error that occurs in response to the test transaction; and

performing a remedial action in response to detecting the error.

11. (Previously Presented) The method of claim 9 further comprising:

providing the test transaction from the test module to an I/O controller coupled to the expansion slot;

providing the test transaction from the I/O controller to a bus bridge;

providing the test transaction from the bus bridge to a system bus;

providing the test transaction from the system bus to a memory controller; and

providing the test transaction from the memory controller to the portion.

12. (Original) The method of claim 11 further comprising:

storing information in the memory in response to the test transaction being a write transaction.

13. (Original) The method of claim 11 further comprising:

in response to the test transaction being a read transaction:

providing information associated with the test transaction from the portion to the memory controller;

providing the information from the memory controller to the system bus;

providing the information from the system bus to the bus bridge;

providing the information from the bus bridge to the I/O controller; and

providing the information from the I/O controller to the test module.

14. (Previously Presented) The method of claim 9 further comprising:

providing the test transaction from the test module to an I/O controller coupled to the expansion slot;

providing the test transaction from the I/O controller to a system controller;

providing the test transaction from the system controller to a memory controller; and

providing the test transaction from the memory controller to the portion.

15. (Currently amended) A computer system comprising:

a processor;

a memory controller coupled to the processor and configured to perform error correction;

a memory coupled to the memory controller;

an input/output (I/O) controller coupled to the memory controller;

an expansion slot coupled to the I/O controller; and

a test module card directly coupled to the expansion slot;

wherein the test module card is configured to obtain access to a portion of the memory from an operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory.

16. (Currently amended) The computer system of claim 15 further comprising:

~~an~~the operating system;

wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory using DMA subsequent to the operating system being booted.

17. (Currently amended) The computer system of claim 15 further comprising:

~~an~~ the operating system;

wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory using DMA during execution of the operating system.

18. (Previously Presented) The computer system of claim 15 wherein the I/O controller provides the read transactions to a system bus.

19. (Previously Presented) The computer system of claim 15 wherein the test module card is configured to cause tests to be performed on the memory using direct memory access (DMA).

20. (Original) The computer system of claim 15 wherein the read transactions comprise direct memory access (DMA) transactions.